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Davison 4-7-23

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signature: _____ Date: October 29, 2004

Applicant(s): K.L. Davison et al.
Case: 4-7-23
Serial No.: 10/722,652
Filing Date: November 26, 2003
Group: 2831
Examiner: Hung V. Ngo

Title: Methods and Apparatus for Integrated Circuit Device Power Distribution via Internal Wire Bonds

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TRANSMITTAL LETTER

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith is the following document relating to the above-identified patent application:

(1) Response to Office Action.

There is no additional fee due in conjunction with the response. In the event of any non-payment or improper payment of a required fee, the Commissioner is hereby authorized to charge or to credit **Ryan, Mason & Lewis, LLP Deposit Account No. 50-0762** as required to correct the error.

Respectfully submitted,

Robert W. Griffith

Date: October 29, 2004

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RESPONSE TO OFFICE ACTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the outstanding Office Action dated July 29, 2004, please consider the following remarks:

REMARKS

The present application was filed on November 26, 2003 with claims 1-20. Claims 1-20 remain pending. Claims 1, 19 and 20 are the pending independent claims.

In the outstanding Office Action dated July 29, 2004, the Examiner rejected claims 1-9, 11 and 13-20 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,727,597 (hereinafter "Taylor").

Applicants acknowledge the indication of allowable subject matter in claims 10 and 12.

In response to the Office Action, Applicants traverse the rejection of claims 1-9, 11 and 13-20.

Independent claim 1 of the present invention recites an integrated circuit device with a die having a peripheral region and an interior region on its top surface. A plurality of bond pads are disposed in the peripheral region of the die, and at least one internal bus is disposed in the interior region of the die. The internal bus distributes power to a plurality of internal node points of the die. At least one bond wire connects at least one of the plurality of bond pads with the at least one internal bus.

Taylor discloses an integrated circuit device having C4 (controlled collapse chip) pads and wire bond pads. Each of the C4 pads is electrically coupled through metal layers and conductive vias to one of the wire bond pads located near the periphery of the integrated circuit device. C4 power connections and ground connections are electrically coupled by traces to one or more wire bond pad power and ground connections, respectively. In order to provide a pad layout that makes it easier to route the electrical connections between the pads, the C4 pads are placed in alignment with the wire bond pads.

Taylor fails to disclose at least one bond wire connecting at least one of a plurality of bond pads, disposed in a peripheral region of the die, with at least one internal bus, disposed in an interior region of the die, as recited in independent claim 1. Instead, in column 2, lines 64-65, Taylor specifically states that "wire bond pads 304 are coupled to the C4 pads 306 through the metal layers 330 and conductive vias 332." Further, in column 3, lines 48-50, Taylor discloses that "the wire bond power connections 350 are coupled to the C4 power buses 360 along a metal trace connecting two of the C4 power connections 340." Therefore, the disclosure of a trace connection instead of a wire bond connection directly teaches away from the invention recited in claim 1 of the present invention.

In the Office Action, the Examiner appears to equate a bond wire and a trace, however the two elements are completely different structures with distinct advantages. While both a bond wire and a trace provide electrical connections, a bond wire is bonded at each end to a bond site through thermal compression, pulse or ultrasonic welding, creating a wire bond profile that loops above the die. A trace is a metal path or line from one element to another in a specific metal layer of the body of the die. Bond wires are purposefully used instead of traces in the present invention for advantageous purposes.

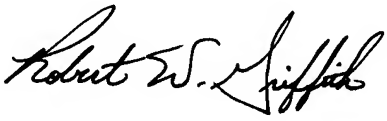
As described on page 4, lines 5-6 of the specification, in conjunction with an illustrative embodiment of the invention, the wire bond connection from peripheral bond pads to bond pads of the internal buses helps to reduce the overall power distribution voltage drop within the device. Further, as described on page 9, lines 19-27, wire bonding allows for sufficient transmission of power to interior regions of the die without increasing the number of metal layers and provides lower resistivity than traditional metal traces, thereby reducing the power distribution voltage drop that normally occurs in metal traces routed from bond pads to the internal buses of the integrated circuit device.

Dependent claims 2-9, 11 and 13-18 are patentable at least by virtue of their dependency on independent claim 1. The patentability of independent claim 1 is described above. Dependent claims 2-9, 11 and 13-18 also recite patentable subject matter in their own right.

Independent claim 19 recites a die configurable for use in an integrated circuit device having a plurality of bond pads, disposed in the peripheral region of the die, and the at least one internal bus, disposed in the interior region of the die, connectable by at least one bond wire. Independent claim 20 recites a method of constructing an integrated circuit device in which at least one peripheral bond pad is wire bonded to at least one internal bus. Therefore, independent claims 19 and 20 are patentable for reasons similar to those presented above with regard to independent claim 1.

In view of the above, Applicants believe that claims 1-20 are in condition for allowance, and respectfully request withdrawal of the §102(e) rejection.

Respectfully submitted,



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